# Full-swing Low Voltage BiCMOS/CMOS Schmitt Trigger

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Abstract - Full-swing low voltage BiCMOS Schmitt trigger which ensures full logic amplitudes in two different ways is described. In this paper full-swing Schmitt trigger circuits have two complementary outputs: BiCMOS (inverting) and CMOS (noninverting). Proposed mathematical model to determine threshold voltages is verified by simulation. Voltage hysteresis depends on supply voltage, MOS transistor threshold voltages and geometry ratio of input MOS transistors and transistors within the positive feedback loop. As this ratio increases from 0.3 to 2, voltage hysteresis changes from  $0.2V_{DD}$  to  $0.54V_{DD}$ .

*Keywords* - low voltage, BiCMOS/CMOS, Schmitt trigger, full-swing, threshold voltages.

#### I. INTRODUCTION

Schmitt trigger is a circuit with a hysteresis shaped transfer characteristic. Its application is very wide, both in mixed signals circuits and in digital ones. As digital circuits, they are usually referred to as Schmitt logic circuits. Those are circuits with standard elementary logic functions (inverter, NAND and NOR) and a hysteresis shaped transfer characteristic [1]. Because of this, Schmitt logic circuits have larger noise immunity than standard circuits. Second advantage is that all output level changes are influenced by positive feedback loop, thus their transfer characteristic are almost ideal (width of the transitional region is neglible), so that noise margin and noise immunity are equal. On the other hand, low frequency signals at the input Schmitt trigger transforms into pulses with very short rise and fall times. Therefore, Schmitt trigger is often used as input circuit of standard MSI or VLSI integrated circuits.

Schmitt logic circuits are often used to design pulse generators. For example, astable multivibrator consists of a Schmitt inverter, a resistor and a capacitor. It is possible to vary RC constant within eight orders of magnitude, so these generators work in a very wide frequency range, from several Hz to several hundreds of MHz. If a current generator is placed instead of the resistor, a simple function generator is achieved. In the same way triangle voltage generators are constructed. Such a voltage, for example, is used as auxiliary voltage within pulse-width modulators. Mixed signals integrated circuits which contain Schmitt trigger are described in [1-3].

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## II. STATIC ANALYSIS

There are more ways to implement CMOS Schmitt triggers [2-4]. In this paper a principle of two different logic threshold voltages of cascode input CMOS transistors, proposed in [5], is used. Other MOS transistors provide optimum operation of bipolar transistors and full-swing at BiCMOS output (Figs. 1 and 2).

Basic circuit of BiCMOS Schmitt trigger (Fig. 1) consists of MOS transistors  $M_{ni}$  (*i*=0,...,4) and  $M_{pj}$  (*j*=0,...,3) and two npn bipolar transistors at the output. Transistors  $M_{n0}$  and  $M_{n1}$ , i.e.  $M_{p0}$  and  $M_{p1}$  ensure the difference of the output level changes thresholds, during positive and negative input voltage change (hysteresis shaped transfer characteristic), and  $M_{n3}$  and  $M_{n4}$  actively turn off transistors  $T_1$  and  $T_2$ , respectively, in static states. CMOS inverters  $I_1$  and  $I_2$ , connected as a latch circuit, besides complement CMOS output  $\overline{Q}$ , ensure full logic swing at the output Q.

Dominant influence to the static transfer characteristic have transistors  $M_{ni}$  and  $M_{pi}$  (*i*=0,1,2). It is optimal when the corresponding pairs of these transistors are symmetric. This means equal constants *k* and threshold voltages of  $M_{n1}$ ,  $M_{n2}$ ,  $M_{p1}$  and  $M_{p2}$  at one side, and  $M_{n0}$  and  $M_{p0}$  on the other side, i.e.:

$$k_{n} = \frac{\mu_{n}\varepsilon_{ox}}{2t_{ox}} \frac{W_{n}}{L_{n}} = k_{p} = \frac{\mu_{p}\varepsilon_{ox}}{2t_{ox}} \frac{W_{p}}{L_{p}},$$

$$k_{n0} = \frac{\mu_{n}\varepsilon_{ox}}{2t_{ox}} \frac{W_{n0}}{L_{n0}} = k_{p0} = \frac{\mu_{p}\varepsilon_{ox}}{2t_{ox}} \frac{W_{p0}}{L_{p0}}$$

$$V_{m} = V_{mi} = |V_{tp}| = |V_{tpi}|, \quad i=0,1,2,$$
(1)

where:  $\mu_n$  and  $\mu_p$  are the mobility of the electrons and the holes,  $\varepsilon_{ox}$  is oxide dielectric constants,  $t_{ox}$  the oxide

thickness and *W* and *L* are width and length of the transistor's channel. In digital circuits it is common to have equal channel lengths for all transistors, which is a specificity of the technology process. Therefore, it is assumed:  $L_{ni}=L_{pi}$ , i=0,...,4. Further, it is assumed:  $k_n=k_{nl}=k_{n2}$  and  $k_p=k_{pl}=k_{p2}$ .

Let input voltage increase from 0 to  $V_{DD}$ . At  $0 \le V_i \le V_{in}$ , transistors  $M_{n1}$ ,  $M_{n2}$ ,  $M_{n3}$ ,  $M_{p0}$ ,  $T_1$  and  $T_2$  are turned off, and  $M_{n0}$ ,  $M_{n4}$ ,  $M_{p1}$ ,  $M_{p2}$  turned on. The Q output is on the high voltage level,  $V_{OH} = V_{DD}$ . Without inverters  $I_1$  and  $I_2$ , transistor  $T_1$  would conduct, thus:  $V_{OH} = V_{DD} \cdot V_{BEI}$ . Because of the latch circuit at the output,  $V_{OH} = V_{DD}$ . As it is:  $V_3 = V_{DD}$ ,  $T_1$  is turned off. Since gate and drain of  $M_{n0}$  hold the same voltage  $(V_{DD})$ , this transistor is in saturation, thus  $V_I = V_{DD} \cdot V_{m0}$ .



Fig. 1. Schmitt trigger with a latch circuit at the output.

For  $V_{tnl} < V_l < V_l + V_{tn2}$ ,  $M_{n2}$  is turned off, and  $M_{n1}$  conducts in saturated region. Also,  $M_{n4}$  conducts until the state change at the output appears. Its influence to transistor's drain current can be taken into account by replacing  $M_{n1}$  and  $M_{n4}$  with one equivalent transistor [1] with twice as large channel length, i.e. constant  $k_{ne}=k_n/2$ . Equalizing drain currents in saturated area of this equivalent transistor and of  $M_{n0}$ , it is obtained:

$$V_{1} = V_{DD} - V_{m0} - \sqrt{W_{n} / 2W_{n0}} \left( V_{i} - V_{m1} \right), \qquad (2)$$

where  $W_n/(2W_{n0}) = (k_n/2)/k_{n0}$ , because of the assumption of equal channel lengths for all transistors. Therefore,  $V_I$  linearly decreases as input voltage increases. Up to  $V_i < V_I + V_{in2}$ ,  $M_{n2}$  is turned off, thus there is no output voltage change, i.e.  $V_o = V_{OH} = V_{DD}$ . When:

$$V_i \ge V_1 + V_{tn2},\tag{3}$$

 $M_{n2}$  conducts, so voltage  $V_3$  will decrease as  $V_1$  increases.  $M_{n0}$  plays the role of source follower, transferring negative change of  $V_3$  to 1, which accelerates  $M_{n1}$  turning on. Thus, positive feedback loop is created, which leads to step change of the outputs Q and  $\overline{Q}$ . Input voltage at which this change happens is the high threshold voltage of the Schmitt trigger,  $V_{TH}$ , and it is calculated from condition  $dV_3/dV_i$ = =-1. The obtained equation is not explicitly solvable. However, it is possible to show that the state of the outputs changes immediately after  $M_{n1}$  starts to conduct. This means that approximate value of  $V_{TH}$  can be obtained from (2) and (3) by equalizing them and changing  $V_i = V_{TH}$ . This yields:

$$V_{TH} = \frac{V_{DD} + \sqrt{(W_n / 2W_{n0})}V_{tn}}{1 + \sqrt{W_n / 2W_{n0}}}$$
(4)

Therefore, the high threshold voltage  $V_{TH}$ , besides of supply voltage  $V_{DD}$  and nMOS transistor threshold voltage  $V_{tn}$ , depends on channel widths ratio of cascode input nMOS transistors and feedback transistor  $M_{n0}$ .

When  $V_i = V_{DD}$ ,  $M_{n1}$ ,  $M_{n2}$ ,  $M_{n3}$  and  $M_{p0}$  are turned on, and  $M_{p1}$ ,  $M_{p2}$ ,  $M_{n4}$ ,  $T_1$  and  $T_2$  are turned off. Inverter  $I_2$ holds voltage at Q output at 0, i.e.  $V_{OL}$ =0V.  $M_{p0}$  is saturated, so  $V_2 = |V_{ip0}|$ . When input voltage decreases,  $M_{p1}$ is turned on first, at  $V_i = V_{DD} + V_{ip1}$ , and then  $M_{p2}$  at:

$$V_i = V_2 + V_{tp2}.$$
 (5)

For  $V_2+V_{tp2} < V_i < V_{DD}+V_{tp1}$ ,  $M_{p1}$  is saturated, so equalizing drain currents of  $M_{p1}$  and  $M_{p0}$  yields:

$$V_2 = \sqrt{W_p / W_{p0}} \left( V_{DD} + V_{tp1} - V_i \right) - V_{tp0}$$
(6)

Immediately after  $M_{p2}$  starts to conduct (Eq. (5)), through  $M_{p0}$ , positive feedback loop is established, thus step change appears at the output from 0 to  $V_{DD}$ . Combining Eqs. (5) and (6) and replacing  $V_i=V_{TL}$ , low threshold voltage of Schmitt trigger is obtained:

$$V_{TL} = \frac{\sqrt{\left(W_p / W_{p0}\right)\left(V_{DD} + V_{tp}\right)}}{1 + \sqrt{W_p / W_{p0}}}$$
(7)

Therefore, the low threshold voltage also, besides  $V_{DD}$  and  $V_{tp}$ , depends on channel widths ratio of pMOS transistors  $M_{p1}$  and  $M_{p0}$ .

#### III. IMPROVED CIRCUIT

As it is already emphasized, output latch circuit with inverters  $I_1$  and  $I_2$  ensures full logic amplitude at BiCMOS output. Since inverter  $I_2$  output is in parallel with BiCMOS output, it increases logic delay, because it decreases charge and discharge currents of the capacitive load. Thus,

transistors of that inverter should be up to about ten times smaller than the other MOS transistors. On the other hand, positive feedback loop, added by the latch, can distort static transfer characteristic under certain conditions.

Output of the improved Schmitt trigger (Fig. 2) with inverter I and transistors  $M_{n4}$  and  $M_{p2}$  does not bring in listed limitations, because BiCMOS output is applied at the input of the inverter I. Since circuit shown in Fig. 2 differs from the one in Fig. 1 only in output stage which enables full-swing, threshold voltages equations are the same.



Fig. 2. Improved BiCMOS Schmitt trigger.

Analytic model is confirmed by simulation, in which BSIM MOSFET [6] and Gummel-Poon bipolar transistor models are used. Transistor parameters of 0.13µm CMOS technology process are used. Threshold voltages of transistor are  $V_m = |V_{tp}| = 0.25$ V. Channel lengths of all MOS transistors are 0.13µm, while nMOS and pMOS channel widths are  $W_n = 2\mu$ m and  $W_p = 6\mu$ m. In Fig. 3 transfer characteristic obtained by simulation at supply voltage  $V_{DD} = 1.25$ V is shown.



Fig. 3. Transfer characteristic obtained by simulation.

In Fig. 4 threshold voltages dependency on geometry ratio of input cascode transistors and feedback transistors

 $M_{n0}$  and  $M_{p0}$  at  $V_{DD}$ =1.25V is shown. Simulation shows high fidelity of the simplified analytic model to calculate thresholds  $V_{TH}$  and  $V_{TL}$ . Expectedly, calculated values are somewhat less than those obtained by simulation, because Eqs. (4) and (7) are input voltages at which  $M_{n2}$  and  $M_{p2}$ start to conduct, respectively. Only after this happens, a positive feedback loop can be established and output change appears. Somewhat more correct, and a lot more complicated analysis, quantitatively would not yield any new results. Actually, it would lose obviousness of the parameters which have the greatest influence. Both analytical model and simulation confirm that supply voltage and  $W_n/W_{n0}$  and  $W_p/W_{p0}$  ratios are dominant in determining  $V_{TH}$  and  $V_{TL}$ . Circuit designer, based on the required voltage hysteresis, from Eqs. (4) and (7) very easily can determine dimensions of the transistors  $M_{n0}$  and M<sub>p0</sub>. Other MOS transistors geometry is determined by a standard procedure for CMOS digital integrated circuits. When input transistors are dimensioned so that their constants k are equal, i.e.  $k_n = k_p$ , ratios changes  $W_n/W_{n0} =$  $W_p/W_{p0}$  from 0.3 to 2, for example, voltage hysteresis can regulate from  $0.2V_{DD}$  to  $0.54V_{DD}$ .



Fig. 4. Threshold voltages dependency on geometry ratio  $W_n/W_{n0} = W_p/W_{p0}$ .

It is known that transfer characteristic of Schmitt trigger is optimal when  $V_{TH}$  and  $V_{TL}$  are symmetric around  $V_i=V_{DD}/2$ . Because of the influence of transistor Mn4, transfer characteristics in Fig. 3 are not symmetric around  $V_{DD}/2$ . Symmetry is obtained when channel width of  $M_{p0}$  is twice as large as of  $M_{p1}$ , i.e.  $W_{p0}=2W_p$ . Then, for  $V_{DD}=2V$ , for example, threshold voltages, based on Eqs. (4) and (7):  $V_{TH}=1.28=V_{DD}/2+0.2V$ , and  $V_{TL}=0.72V=V_{DD}/2-0.2V$ . Therefore, transfer characteristic is symmetric with voltage hysteresis  $V_H=V_{TH}-V_{TL}=0.56V$ . Symmetry is verified by simulation (Fig. 5) at following parameters:  $V_{DD}=2V$  and  $W_{p0}=12\mu$ m. Other parameters are the same as those used for Fig. 3.



Fig. 5. Transfer characteristic obtained by simulation at  $W_{p0}=2W_p$  and  $V_{DD}=1V$ .

Dependency of propagation time on ratios  $W_n/W_{n0} = W_p/W_{p0}$ , with capacitive load at the output  $C_L = 5\text{pF}$  and  $V_{DD} = 2\text{V}$  and  $V_{DD} = 1.5\text{V}$ , is shown in Fig. 5. Change sensitivity of  $t_p$  is less in area  $W_n/W_{n0} = W_p/W_{p0} > 1$ . The same stands for change sensitivity of  $V_{TH}$  and  $V_{TL}$  (Fig. 4). Increasing ratio  $W_n/W_{n0} = W_p/W_{p0}$ , both logic delay and voltage hysteresis are decreased. As  $V_H$  decreases, noise immunity decreases. Thus, to achieve a compromise between small propagation time and high noise immunity, it needs to be  $W_n/W_{n0} = W_p/W_{p0} = 1$ .

Transistors of the input inverter I are defined based on the required strength of CMOS output. If this output is not used, the same geometry of transistors, as of those at the input, is recommended. If small hysteresis is required, output inverter should be dimensioned so that its threshold voltage is less than  $V_{DD}/2$ .



Fig. 6. Propagation time versus  $W_n/W_{n0} = W_p/W_{p0}$ , with capacitive load  $C_L$ =5pF and  $V_{DD}$ =2V and  $V_{DD}$ =1.5V.

# IV. CONCLUSION

Application of the Schmitt trigger in Fig. 2 is recommended since it has better static stability and less propagation time. Reliability of operation is ensured in a wide range of supply voltages. Simulation shows that the circuit operates even at  $V_{DD}$ =0.7V. However, the influence of bipolar transistors is neglible for  $V_{DD}$ <1V, so appropriate CMOS solutions are recommended for this area of  $V_{DD}$ . Voltage hysteresis, besides on supply voltage and MOS transistors threshold voltages, depends on geometry ratios of input cascode MOS transistors and feedback ones. Changing this ratio from 0.3 to 2, voltage hysteresis can be adjusted within limits from  $0.2V_{DD}$  to  $0.54V_{DD}$ . However, ratio 1 is optimal choice among two opposite demands: less propagation time and greater voltage hysteresis, where  $V_H$ =0.25 $V_{DD}$ .

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